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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HUYNH, KIM T	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,076	MARTIN ET AL.	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 5 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claims 5. See MPEP § 608.01(n). Accordingly, the claim 5 not been further treated on the merits. Correction is appropriate required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thurlo et al. (Pub. No. US2004/0044817) in view of Brown (US Patent 6,728,808) As per claims 1 and 5, Thurlo discloses an apparatus, comprising:

a peripheral component interconnect (PCI) standard hot-plug controller (SHPC) having: (paragraph 32-35, ie HPC)

a first register coupled to store a first and a second PCI slot operation command, the second PCI slot operation command being different from the first PCI slot operation command; and [paragraph 35-39, ie controller maps slot instructions into a memory register from which the instruction will be executed, each instruction per operation per slot]

Thurlo discloses all the limitations as above except a second register coupled to the first register, the second register to store a first value and a second value for a timing parameter in a signal sequence for execution of the first and second PCI slot operation commands, respectively, the second value being different from the first value. However, Brown discloses the timing value stored within programmable retry value register can represent any specific interval of time. (col.9, lines 3-32)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Brown's teaching into Thurlo's system as so for optimizing transaction signal retires between a PCI bus master device and a target device communicatively coupled by a PCI bus. (col.2, lines 34-39)

As per claims 9, discloses an apparatus, comprising:

a peripheral component interconnect (PCI) standard hot-plug controller (SHPC) having: (paragraph 32-35, ie HPC)

a first register coupled to store a first and a second PCI slot operation command, the second PCI slot operation command being the same as the first PCI slot operation command; and [paragraph 35-39, ie controller maps slot instructions into a memory register from which the instruction will be executed, each instruction per operation per slot]

Thurlo discloses all the limitations as above except a second register coupled to the first register, the second register to store a first value and a second value for a timing parameter in a signal sequence for execution of the first and the second PCI slot operation commands, respectively, the second value being different from the first value. However, Brown discloses the timing value stored within programmable retry value register can represent any specific interval of time. (col.9, lines 3-32)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Brown's teaching into Thurlo's system as so for optimizing transaction signal retires between a PCI bus master device and a target device communicatively coupled by a PCI bus. (col.2, lines 34-39)

As per claims 13, 18,23, discloses an article of manufacture including a machine-accessible medium having data that, when accessed by a machine, cause the machine to perform the operations comprising:

receiving at a second register in a standard hot-plug controller (SHPC) a first peripheral component interconnect (PCI) slot operation command; [paragraph 35-39, ie controller maps slot instructions into a memory register from which the instruction will be executed, each instruction per operation per slot]

Thurlo discloses all the limitations as above except receiving at a first register in the SHPC a first value for a timing parameter in a signal sequence for

execution of the first PCI slot operation command; executing the first PCI slot operation command using the signal sequence and the first value for the timing parameter; receiving at the second register a second PCI slot operation command different from the first PCI slot operation command; and receiving at the second register a second value different from the first value for the timing parameter in the signal sequence for execution of the second PCI slot operation command. However, Brown discloses the system includes a retry timer circuit coupled to the PCI bus to variable the timing value stored within programmable retry value register can represent any specific interval of time. (col.9, lines 3-32)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Brown's teaching into Thurlo's system as so for optimizing transaction signal retires between a PCI bus master device and a target device communicatively coupled by a PCI bus. (col.2, lines 34-39)

As per claims 2, 6,10,14,19,24, Brown discloses wherein the timing parameter is a time delay between assertion of a signal to control a power state of a target PCI slot and assertion of a signal to control connection of a PCI clock to the target PCI slot. (col.2, lines 40-51)

As per claims 3, 7, 11,15,20, 25, Brown discloses wherein the timing parameter is a time delay between assertion of a signal to control connection of a PCI clock

to a target PCI slot and assertion of a signal to control connection of at least one bus signal to the target PCI slot. (col.2, lines 40-51)

As per claims 4, 8, 12, 16, 21, 26, Brown discloses wherein the timing parameter is a time delay between assertion or de-assertion of a signal to control a power state of a target PCI slot and assertion of a signal indicating completion of the first or second PCI slot operation command. (col.2, lines 40-51)

As per claim 5(as best as understood), Thurlo discloses wherein the first and second first and a second PCI slot operation commands are a command to apply power to the target PCI slot, to enable the target PCI slot, to disable the target peripheral card interconnect slot, or to change the speed of the PCI bus. [paragraph 35-39]

As per claims 17, 22, 27, Brown discloses wherein the timing parameter is a time delay between de-assertion of a signal to control a power state of at least one target PCI slot and assertion of a signal indicating completion of the first or second PCI slot operation command. (col.2, lines 40-51)

As per claim 28, Thurlo discloses a system, comprising:

a peripheral component interconnect (PCI) standard hot-plug controller (SHPC) having a first register coupled to store a first and a second PCI slot

operation command associated with a first and a second target PCI slot, the second target PCI slot being different from the first target PCI slot, and a second register coupled to the first register, the second register to store a first value [paragraph 35-39, ie controller maps slot instructions into a memory register from which the instruction will be executed, each instruction per operation per slot] ; and a static random access memory (SRAM)(fig.1, 126 ie flash memory or cache 132) coupled to the microprocessor(fig.1, 110 I/O controller or processor 102).

Thurlo discloses all the limitations as above except a second value for a timing parameter in a signal sequence for execution of the first and the second PCI slot operation commands, respectively, the second value being different from the first value; However, Brown discloses the timing value stored within programmable retry value register can represent any specific interval of time. (col.9, lines 3-32)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Brown's teaching into Thurlo's system as so for optimizing transaction signal retires between a PCI bus master device and a target device communicatively coupled by a PCI bus. (col.2, lines 34-39)

As per claim 29. Thurlo discloses the system further comprising a memory controller (fig.1, 104, ie memory controller) coupled to the memory(fig.1, 106 ie memory).

As per claim 30, Thurlo discloses the system further comprising a software driver coupled to provide the first and the second PCI slot operation commands.[paragraph 32]

Conclusion

4. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached at (571)272-3676 or via e-mail addressed to [rehana.perveen@uspto.gov].*

The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Kim Huynh

March 16, 2006

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
3/16/06